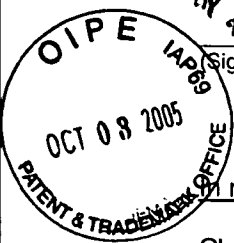


I hereby certify that this correspondence is being deposited via first class mail with the United States Postal Service addressed to : Commissioner of Patents and Trademarks, Alexandria, VA 22313, on September 29, 2005.
The applicant and/or attorney requests the date of deposit as the filing date.

Depositor: ~~Robert Faber~~ Nicole Barrese

IFW



Robert Faber 9-29-05
(Signature & date)

Nicole Barrese 9/29/05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of _____:

September 26, 2005

Cheng, et al. _____:

Group Art Unit: 2812

Serial No: 10/710,608 _____:

Examiner: Tara Washington

Filed: 7/23/04 _____:

International Business Machines Corporation
2070 Route 52
Hopewell Junction, NY 12533

TITLE: Patterned Strained Semiconductor Substrate and Device

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

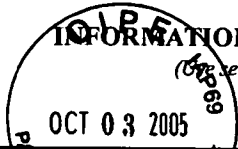
Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the US and non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Cheng, et al.

By Joseph P. Abate 9-26-05
Joseph P. Abate
Registration No. 30,238
Telephone No. 845-894-4633

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|---|---|----------------------------------|
|  <p>INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)</p> | Docket Number (Optional) FIS920040150US1 | Application Number 10/710,608 |
| | Applicant(s) Cheng, et al. | |
| | Filing Date 7/23/04 | Group Art Unit 2812 |

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| | | US 2002/0074598 A1 | 6-20-02 | Doyle, et al. | | | |
| | | US 2002/0086472 | 7-4-02 | Roberds, et al. | | | |

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| | REF | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | Translation | |
|--|-----|-----------------|---------|---------|-------|----------|-------------|----|
| | | | | | | | YES | NO |
| | | JP64-76755 | 03-1989 | Japan | | | | |
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| | | Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si n-MOSFETs". International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998. |
| | | Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs." 2002 Symposium on VLSI Technology Digest of Technical Papers, IEEE, pp. 98-99. |

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

FIS920040150US1

Application Number

10/710,608

Applicant(s)

Cheng, et al.

Filing Date

7/23/04

Group Art Unit

2812

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F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Application." International Electron Devices Meeting, 23.5.1, IEEE, April 2000.

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| | | 5,310,446 | 5-10-94 | Konishi, et al. | | | |
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| | | Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design." International Electron Devices Meeting, 10.7.1, IEEE, April 2000. |
| | | A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement." International Electron Devices Meeting, IEEE, March 2001. |

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| | | 5,557,122 | 9-17-96 | Shrivastava, et al. | | | |
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| | | K. Ota, et al., "Novel Locally Strained Channel Technique for High Performance 55nm CMOS." International Electron Devices Meeting, 2.2.1, IEEE, February 2002. |
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| | | C.J. Huang, et al., "Temperature Dependence and Post-Stress Recovery of Hot Electron Degradation Effects in Bipolar Transistors." IEEE 1991 Bipolar Circuits and Technology Meeting 7.5, pp. 170-173. <div style="text-align: center;">no date</div> |

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| | | 5,683,934 | 11-4-97 | Candelaria | | | |
| | | 5,840,593 | 11-24-98 | Leedy | | | |
| | | 5,861,651 | 1-19-99 | Brasen, et al. | | | |
| | | 5,880,040 | 3-9-99 | Sun, et al. | | | |
| | | 5,940,716 | 8-17-99 | Jin, et al. | | | |

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| | | 5,946,559 | 8-31-99 | Leedy | | | |
| | | 5,960,297 | 9-28-99 | Saki | | | |
| | | 5,989,978 | 11-23-99 | Peidous | | | |
| | | 6,008,126 | 12-28-99 | Leedy | | | |

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| | | 6,025,280 | 2-15-00 | Brady, et al. | | | |
| | | 6,046,464 | 4-4-00 | Schetzina | | | |
| | | 6,066,545 | 5-23-00 | Doshi, et al. | | | |
| | | 6,090,684 | 7-18-00 | Ishitsuka, et al. | | | |
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| | | H.S. Momose, et al., "Analysis of the Temperature Dependence of Hot-Carrier-Induced Degradation in Bipolar Transistors for Bi-CMOS." IEEE Transactions on Electron Devices, vol. 41, no. 6, June 1994, pp. 978-987. |

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| | | 6,117,722 | 9-12-00 | Wuu, et al. | | | |
| | | 6,133,071 | 10-17-00 | Nagai | | | |
| | | 6,165,383 | 12-26-00 | Chou | | | |
| | | 6,221,735 | 4-24-01 | Manley, et al. | | | |
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| | | J.C. Bean, et al., "GEx Si 1-x/Si Strained-Layer Superlattice Grown by Molecular Beam Epitaxy". J. Vac. Sci. Technol. A 2(2), Apr.-June 1984, pp. 436-440. |

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| FOREIGN PATENT DOCUMENTS | | | | | | | | |
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INFORMATION DISCLOSURE CITATION*(Use several sheets if necessary)*

Docket Number (Optional)

FIS920040150US1

Application Number

10/710,608

Applicant(s)

Cheng, et al.

Filing Date

7/23/04

Group Art Unit

2812

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| INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i> | Docket Number (Optional) FIS920040150US1 | Application Number 10/710,608 |
| | Applicant(s) Cheng, et al. | |
| | Filing Date 7/23/04 | Group Art Unit 2812 |

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